## REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 30, 2003, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-2, 4-14, 26-32, and 35-39 are now pending in this application.

### *§103 Rejection of the Claims*

Claims 1-2, 4-5, & 7-10 were rejected under 35 USC § 103(a) as being unpatentable over Nakanishi (U.S. 5,145,797) in view of Lisenker et al. (WO 94/19829) and further in view of admitted prior art. The Nakanishi reference describes a method for reducing electron leakage in EPROMs and EEPROMs that includes doping side portions of a floating gate and control gate with phosphorus. There is no suggestion that any other treatment would accomplish the result. Furthermore, the method employs annealing in the context of ion implantation, as described in col. 5, lines 42-48. "ion implantation and annealing are performed to form impurity diffusion layers 24a and 24b forming the source and drain regions on the surface of the semiconductor substrate 2 by self-alignment with the gates..." Furthermore, as acknowledged by the Examiner, the Nakanishi reference does not describe providing a semiconductor surface and heating the surface in the presence of a hydrogen isotope as is claimed.

The Examiner is combining Nakanishi with Lisenker et al. to reject claims 1-2, 4-5, and 7-10. However, in order to combine references, there must be motivation to combine. Nakanishi is doping side portions of a floating gate and control gate with phosphorus and annealing to form doped layers. There is no motivation for Nakanishi to employ deuterium at all because Nakanishi is employing phosphorus doping to solve an electron leakage problem. There is no suggestion in Lisenker as to how one would treat an EEPROM or EPROM doped with phosphorus in order to reduce random single bit data loss because Lisenker does not address this problem. Thus, the Applicant asserts that there is no motivation to combine the Nakanishi and Lisenker, or, what the Examiner refers to as "admitted prior art" references and even if they were combined it is not clear what would be accomplished in the combination. There is no direction in either reference as to what portion of the EPROM or EEPROM, if any, should be treated with deuterium in order to reduce random electron leakage. There is no suggestion that treating with

deuterium would reduce electron leakage. Instead, the combination shows a use of ion doping with phosphorus. It is not clear in Lisenker that an addition or substitution of deuterium in the doping step or any other step would be effective in reducing electron leakage in an EPROM or EEPROM. The Examiner is using the present invention as a guide to combine these references to achieve a particular outcome. Lisenker did not contemplate the outcome and Nakanishi describes a very different approach to treatment.

Claim 6 was rejected under 35 USC § 103(a) as being unpatentable over Nakanishi (U.S. 5,145,797) in view of Lisenker et al. (WO 94/19829) and further in view of admitted prior art as applied to claims 1-2, 4-5, & 7-10 above, and further in view of Nakajima et al. (U.S. 5,397,724). Claim 6 describes the "method of claim 1 and further comprising exposing the semiconductor layer, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature." The Examiner uses a complex argument while acknowledging that neither Lisenker nor Nakajima describe the features of this claim. As discussed above, the Nakajima reference does not include motivation to combine with Lisenker because the problem and solution described in Nakajima are not addressed in Lisenker. Further, there is no evidence in Nakajima that ammonia is used as part of the process, much less that a semiconductor is exposed, sequentially, "to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature." This is a presumption of the Examiner, based upon hindsight gained from the present invention.

Claims 11-14 rejected under 35 USC § 103(a) as being unpatentable over Nakanishi (U.S. 5,145,797) in view of Lisenker et al. (WO 94/19829) and further in view of admitted prior art as applied to claims 1-2, 4-5, & 7-10 above, and further in view of Sheu (U.S. 4,840,917). Here also, the Examiner acknowledges that the Nakanishi reference does not disclose the claimed steps, but argues that the Nakanishi reference would have performed the passivation claimed. However, the Nakanishi reference does not perform the passivation and there is no suggestion to do so. The Examiner is using the present invention as a guide to combine references.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6976 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 30 July 03

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 30th day of July, 2003

Amy Moriarty
Name

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Signature